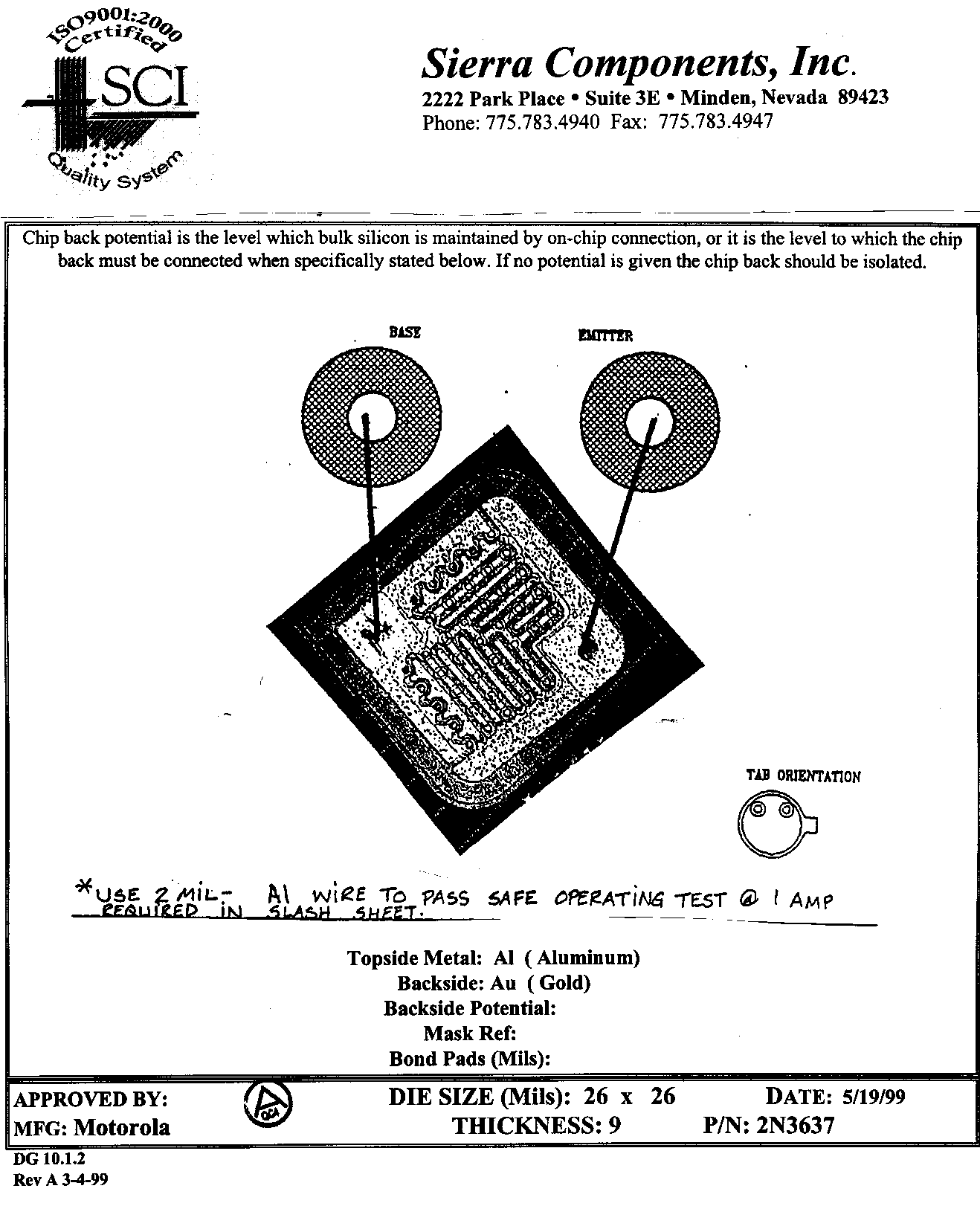
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**BASE**

**EMITTER**

**.025”**

**.025”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .026” X .026” DATE: 10/7/21**

**MFG: MOTOROLA THICKNESS .009” P/N: 2N3637**

**DG 10.1.2**

#### Rev B, 7/1